

ABSTRACT OF THE DISCLOSURE

One embodiment of a distributed memory module cache includes tag memory and associated logic implemented at the memory controller end of a memory channel. The memory controller is coupled to at least one memory module by way of a point-to-point interface. The data cache and associated logic are located in one or more buffer components on each of the memory modules. One intended advantage of this example embodiment is the ability to read a current line of data out of a memory module DRAM and to load the next cache line of data into the memory module data cache. This allows the utilization of excess DRAM interconnect bandwidth while preserving limited memory bus bandwidth.